Hi3798M V200 Brief Data Sheet

Key Specifications

High-Performance CPU

- Quad-core 64-bit high-performance ARM Cortex A53
- Integrated multimedia acceleration engine NEON
- Hardware Java acceleration
- Integrated hardware floating-point coprocessor

3D GPU

- Integrated high-performance multi-core GPU Mali 450
- OpenGL ES 2.0/1.1 and OpenVG 1.1

Memory Control Interfaces

- DDR3/3L/4 SDRAM interface, maximum 32-bit data width
- SPI NOR flash interface
- SPI NAND flash interface
- Asynchronous/Synchronous NAND flash interfaces
  - SLC/MLC flash memory
  - Maximum 64-bit ECC
- eMMC 5.0 flash interface

Video Decoding (HiVXE 2.0 Processing Engine)

- H.265/HEVC Main/Main 10 profile@level 5.1 high-tier, maximum 4K x 2K@60 fps 10-bit decoding
- H.264/AVC BP/MP/HP@level 5.1, H.264/AVC MVC, maximum 4K x 2K@30 fps decoding
- Maximum 4K x 2K@60 fps 10-bit VP9 decoding
- Maximum 1080p@60 fps VP6/8 decoding
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- Maximum 1080p@60 fps MPEG-1 decoding
- Maximum 1080p@60 fps MPEG-2 SP@ML, MP@HL decoding
- MPEG-4 SP@levels 0−3, ASP@levels 0−5, GMC, short header format, maximum 1080p@60 fps decoding
- AVS baseline profile@level 6.0, AVS-P16 (AVS+), maximum 1080p@60 fps decoding
- VC-1 SP@ML, MP@HL, AP@levels 0−3, maximum 1080p@60 fps decoding

Image Decoding

- JPEG decoding, maximum 64 megapixels
- PNG decoding, maximum 64 megapixels

Video and Image Encoding

- H.265 MP@level 5 main tier and H.264 BP/MP/HP@level 4.2 video encoding, maximum 1x1080p@30 fps or 2x720p@30 fps encoding
- VBR or CBR mode
- Low-delay encoding
- Encoding of multiple ROIs

Audio Encoding/Decoding

- MPEG L1/L2
- Dolby Digital/Dolby Digital Plus decoder-converter
- Dolby True HD decoding
- DTS HD/DTS M6 decoding
- Dolby Digital/DTS transparent transmission
- Dolby ATMOS
- AAC-LC and HE AAC V1/V2 decoding
- APE, FLAC, Ogg, AMR-NB, and AMR-WB decoding
- G.711 (u/a) audio decoding
- Dolby MS11 decoding and audio effect
- G.711 (u/a), AMR-NB, AMR-WB, and AAC-LC audio encoding
- HE-AAC transcoding DD (AC3)

TS Demultiplexing/PVR

- Multi-channel TS processing
- Various descrambling algorithms of the DVB
- Recording of scrambled and non-scrambled streams

Security Processing

- Advanced CA
- Downloadable CA
- TVOS security mechanism
- Secure boot, secure storage, and secure upgrade
- DRM and hardware watermark
- HDCP 2.2/1.4 protection for HDMI outputs

Graphics and Display Processing (Imprex 2.0 Processing Engine)

- Dolby Vision, HDR10, and HLG
- Conversion from HDR to SDR
- Hardware overlaying of multi-channel graphics and video inputs
- Multiple graphics layers and video layers
- Multi-order vertical and horizontal scaling of videos and graphics; free scaling
- Screen mirroring and video rotation
- Full-format 3D video processing and display
- Enhanced TDE
- Anti-aliasing, anti-flicker, enhancement of image colors and luminance, NR, DEI, sharpening, as well as adjustment of the luminance, chrominance, contrast, and saturation
- Ultra-low-delay video processing

Audio/Video Interfaces

- PAL, NTSC, and SECAM standard outputs, and forcible standard conversion
- Aspect ratio of 4:3 or 16:9, forcible aspect ratio conversion, and free scaling
- 4Kp@60fps/50fps/30fps/25fps, 1080p@60fps/50fps/30fps/24fps, 1080i@60fps/1080i@50fps, and 720p/576p/576i/480p/480i outputs
- HD and SD outputs
- One HDMI 2.0b TX with HDCP 2.2 output, maximum 4K x 2K@60 fps
- Analog video interfaces
  - One CVBS interface
  - One embedded VDAC
  - VBI
- Audio interfaces
  - Audio-left and audio-right outputs
  - S/PDIF interface
  - One embedded ADAC
  - One I^2S/PCM digital audio input/output interface
  - HDMI audio output interface

Peripheral Interface

- Two USB 2.0 host ports

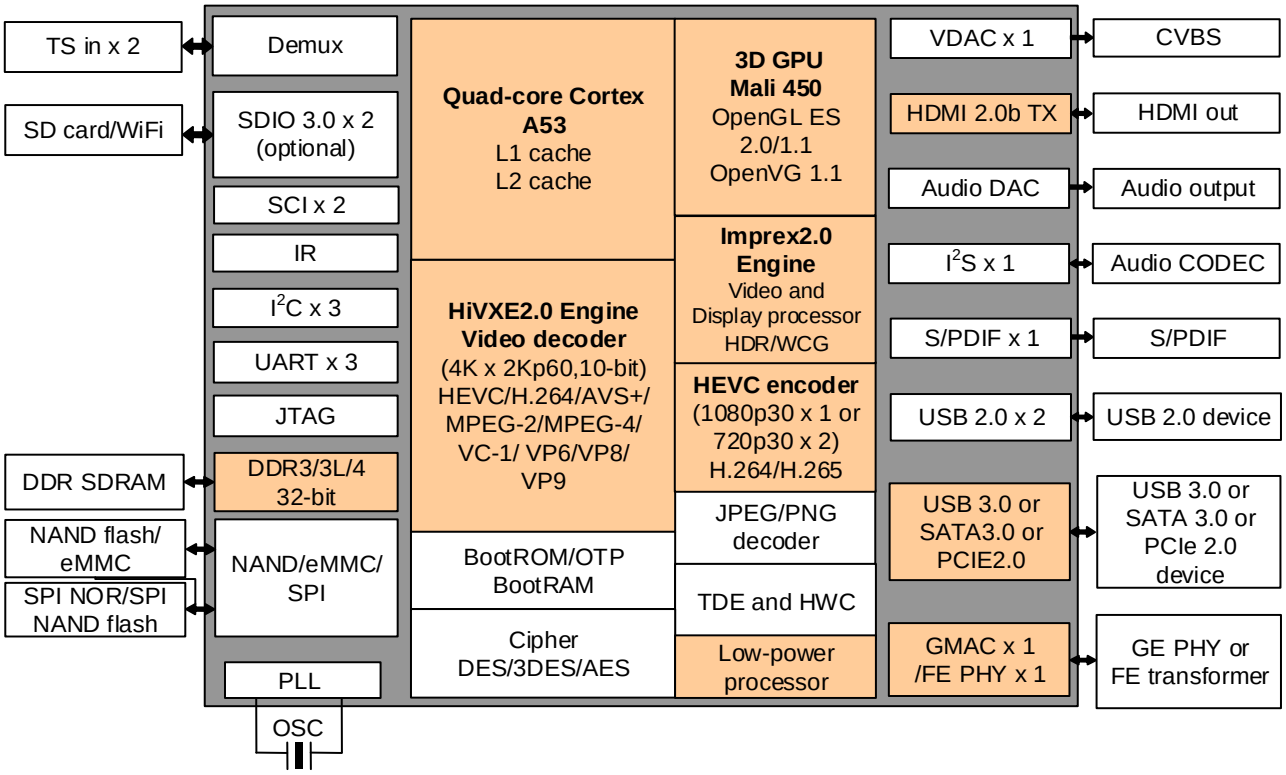
Hi3798M V200 Brief Data Sheet

- One USB 3.0 host port (optional), compatible with USB 2.0 port
- One SATA 3.0 interface (optional)
- One PCIe 2.0 interface (optional)
- One 1000 Mbit/s Ethernet port or one 100 Mbit/s Ethernet port, one GMAC and one FE PHY integrated
- Two 4-bit SDIO 3.0 interfaces (optional)
- Three UART interfaces
- Two SCI Controllers
- One IR receiver
- One LED and keypad control interface
- Three I^2C interfaces
- Multiple groups of GPIO interfaces
- One embedded POR

Others

- Various boot modes
- Boot program download and execution over a serial port or USB port
- Passive standby low-power design, integrated standby processor, supporting various low-power modes and less than 30 mW standby power consumption
- BGA 14 mm x 14 mm (0.55 in. x 0.55 in.) package, 2-layer PCB supported

Functional Block Diagram



Hi3798M V200 is a full-4K high-performance SoC that supports 4Kp60 decoding for the Internet Protocol television (IPTV)/over-the-top (OTT) STB markets. It integrates the 4-core 64-bit high-performance Cortex A53 processor and multi-core high-performance 2D/3D acceleration engine. Besides, it supports H.265 4K x 2K@P60 10-bit ultra-HD video decoding, high-performance H.265 HD video encoding, HDR video decoding and display, Dolby, and DTS audio processing. Hi3798M V200 also provides rich internal peripheral interfaces, such as USB 2.0, USB 3.0, SDIO 3.0, and PCIe 2.0 interfaces. These features help customers implement full-4K service deployment, and enable Hi3798M V200 to provide the best user experience in the industry in terms of picture quality, stream compatibility, video playback smoothness, and STB performance and meet the requirements of continuously increasing value-added services such as video communication, karaoke, cloud game, and multi-screen interaction.

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Acronyms and Abbreviations

ADAC	audio digital-to-analog converter
AES	advanced encryption standard
AVS	audio video standard
BOM	bill of material
CA	conditional access
CBR	constant bit rate
CSC	color space conversion
CVBS	composite video broadcast signal
DES	data encryption standard
ECC	error-correcting code
EPG	electronic program guide
GPIO	general-purpose input/output
GPU	graphics processing unit
HDMI	high-definition multimedia interface
I^2C	inter-integrated circuit
IR	infrared
I^2S	inter-IC sound
JPEG	Joint Photographic Experts Group
MPEG	Moving Picture Experts Group
NTSC	National Television System Committee
PBGA	plastic ball grid array
PCB	printed circuit board
PID	packet identifier
QFP	quad flat package
SCI	smart card interface
S/PDIF	Sony/Philips digital interface
SPI	serial peripheral interface
STB	set-top box
SVP	secure video path
TDE	two-dimensional engine
UART	universal asynchronous receiver transmitter
VBI	vertical blanking interval
VBR	variable bit rate
VDAC	video digital-to-analog converter